# Upgrade scenarios for OPS networks

Jan Cheyns, Didier Colle, Chris Develder, Erik Van Breusegem, Mario Pickavet, Piet Demeester

*Abstract*— **Optical Packet Switching can cope well with the bursty nature of data traffic that is becoming predominant. OPS nodes will be used in a network, where traffic demand will show a growth evolution. In stead of immediately installing a large OPS node that is only sparsely used in the first years, we prefer solutions allowing the switch to grow as traffic demand grows. We look into modular, multistage solutions for two well-known OPS node designs. We evaluate the cost evolution for different design choices, using several scenarios. We show that multistage OPS node designs can result in cheaper, modular upgradeable designs.**

*Index Terms*— **Techno-economics, Optical Communication, Packet Switching.**

## I. Introduction

OPTICAL networks have been undergoing fast and vast changes and at the dawn of the 21st century they still stand before large evolutions. On the one hand there is the circuit switched ASON technology, allowing for automatic setup of lightpaths and a dynamic and flexible Optical Transport Network layer [1]. On the other hand important research topics are packet switched optical networking techniques such as Optical Packet Switching (OPS) [2] and Optical Burst Switching (OBS) [3]. These technologies have a more efficient bandwidth usage through statistical multiplexing.

An important factor in every network architecture is the dimensioning of the capacity in the network and the switching capacity of the individual nodes. This traffic is not static by nature and continues to grow. Growth estimates themselves are always difficult and have been known to both under- and overestimate the growth greatly. Some relevant info on traffic and growth are found in [4]. One thing however is sure: switching nodes must be able to grow together with the traffic, and preferably in an economic (i.e. cost efficient) way.

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In previous work we tried to compare the costs of several node architectures [5]. We now want to go deeper into the cost evolution for OPS nodes, when taking the traffic growth into account. We will use multistage OPS node architectures [6], as these are interesting from an upgrading perspective.

In Section II we start by describing two commonly used OPS node architectures. We continue by shortly discussing the multistage variants in Section III. In IV we then look at such multistage architectures from an upgrading point of view. Section V continues by describing the methods used in this paper, different scenarios are discussed in VI, leading to our conclusions in VII.

## II. OPS Node Architectures

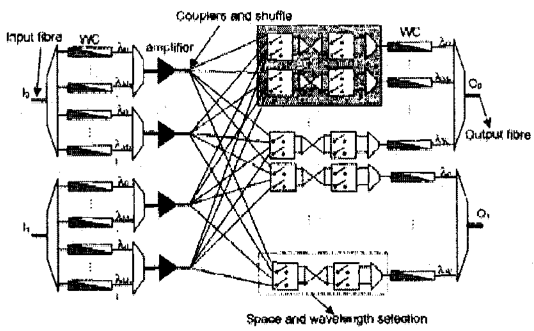


Fig. 1 General Broadcast & Select node design, using SOAs.

In this paper we will use $F$ to denote the number of incoming fibres and $W$ the number of wavelengths on each fibre. We will only look into symmetrical switches, i.e. where the number of outgoing fibres is also equal to $F$.

### A. The SOA based Broadcast & Select architecture

The general Broadcast & Select (B&S) node has a central part surrounded by two (fixed wavelength output) Wavelength Converter stages (WC in Fig. 1). These stages do the conversion from the external wavelengths

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(the ones on the in- and output fibres) to the internal wavelengths. We denote the number of internal wavelengths by $M$. In the multiplex and amplify stage of the switch $M$ (16 in Fig. 1) internal wavelengths are multiplexed into a multi-wavelength signal, which is amplified. This amplified signal than goes through a (power) splitter that evenly distributes the signal over the inputs of the space and wavelength selection stage. The active components in this switching block are Semiconductor Optical Amplifiers (SOA). For each output wavelength, two switching stages are present: the first selects one of the $F$ input fibres, while the second one selects a single wavelength among the $W$ available ones. At the end the (fixed wavelength output) Wavelength Converters make sure the output signals are all on correct wavelengths.

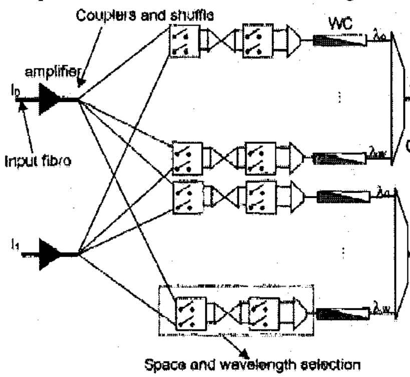

Fig. 2 B&S switch design where internal and external wavelengths are the same.

A special case of the B&S switch design occurs when the number of internal wavelengths is the same as the number of external wavelengths. In this case the Wavelength Converters at the input can be removed from the design. The resulting architecture is shown in Fig. 2, which clearly shows the simplification over Fig. 1.

### *B. The AWG based architecture*

Another class of OPS nodes is based on AWGs. An AWG is a passive optical component with $N$ in- and output ports. Light that enters at one of the input ports exits at a certain output port, depending on the wavelength of the signal. This principle will become clear as we explain the functioning of the basic AWG based OPS node. We will not discuss these node architectures in detail, only basic information on the way they work will be given, more details can found in [7].

In its simplest design there is a (fully optical) Tuneable Wavelength Converter (TWC) before each of the $N$ input ports of the AWG allowing to change the wavelength of the incoming signal, shown in Fig. 3. As we can thus manipulate the wavelength on the AWG input port we can control on which AWG output port this signal will exit. On Fig. 3 two examples are given: a signal is incoming on AWG input port 4. If it is on $\lambda_0$ it will exit on fibre $O_0$, if it is on $\lambda_1$ it will exit on $O_1$. The AWG output ports are coupled together into the output fibre.

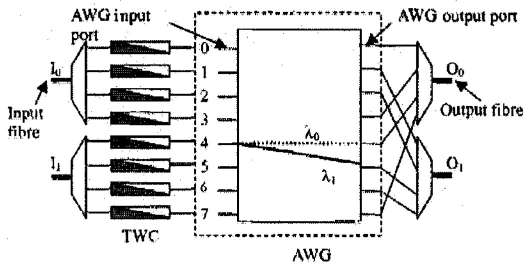

Fig. 3 Basic AWG based design: internal blocking present.

In the design of Fig. 3 the TWCs have an output range of $W$: the same $W$ wavelengths can be set as the ones that can be present on the input fibres. The consequence of this condition is that the node shows some blocking. This blocking can be reduced substantially in synchronous operation [8] [9], but not in asynchronous operation [10].

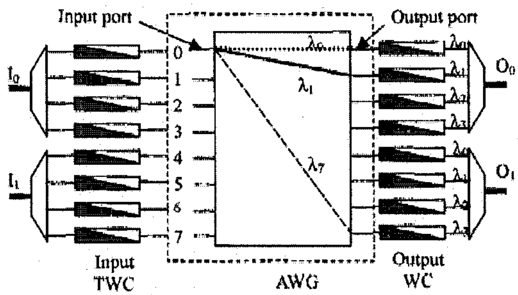

Fig. 4 Non-blocking version of the AWG based design: no more internal blocking present.

The basic node design suffers from blocking, clearly a disadvantage. Modifications can make the node non-blocking, leading to the design of Fig. 4. The input TWCs have an enlarged range ($F.W$), i.e. each input TWC is able to transmit from $\lambda_0$ up to $\lambda_{F.W-1}$. Thus any AWG output port can be accessed from any AWG input port, as shown in Fig. 4 for AWG input port 0. This results in a strictly non-blocking design: regardless of the current setting of the switch a free AWG input port can be connected with a free AWG output port. Comparing Fig. 4 with Fig. 3 there are now also output wavelength converters present. Indeed, on the output fibre only $\lambda_0$ to $\lambda_{W-1}$ are allowed. Internally the switching node however has $F.W$ possible wavelengths, thus output conversion is necessary. The output wavelength of these converters can be fixed (output wavelength shown on Fig. 4), so a Fixed Wavelength Converter (FWC) can be used. A FWC converts any incoming wavelength into a predefined (thus fixed) wavelength, so it is simpler and cheaper than a TWC.

## III. Multistage Node Architectures

Over 50 years ago Clos presented his paper on multistage switch architectures [11], which are still very actual today [6]. Next to the well-known cost advantage, an extra pro of using multistage Clos architectures is that they can have a modular build, which allows the switch to grow as the demand grows, without having to install a full-blown (overdimensioned) node from the beginning. We will present the Clos 3-stage variants for OPS of the above described designs, and shortly motivate their interest form cost point of view. In subsection IV.B we deal with a modification of the Clos design, which can yield even better modular designs.

### A. *The SOA based Broadcast & Select architecture*

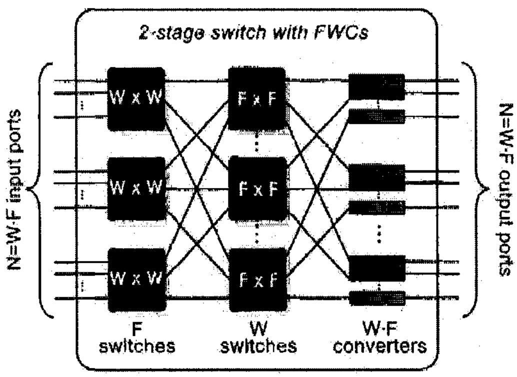


Fig. 5 Two stage design for a B&S switching node.

Fig. 5 shows a 2-stage Clos design based on the B&S switch design. The design shows a rearrangeable non-blocking node architecture [12]: the number of middle stages is equal to the size of the input blocks. The WxW and FxF blocks are blocks as the ones shown in Fig. 2. In the classic 3-stage Clos design there is also a switching stage at the output (a $3^{rd}$ stage). In Fig. 5, this is replaced with Fixed Wavelength Converters.

In OPS, part of the solution to contention resolution is to employ wavelength conversion: when two or more packets need to be switched to the same outgoing fibre, one or more of them may be converted to another wavelength to allow their simultaneous transmission on the output fibre. So we are not interested on which exact wavelength channel the packet is put, we only want it on the correct output fibre. The only limitation is that no two packets on the same output fibre can have the same wavelength. This allows a simplification of the design: if we choose to have all outputs of a $3^{rd}$ stage switch going to the same output fibre, we can replace the $3^{rd}$ stage switch by Fixed output Wavelength Converters (FWCs). Thus, we obtain a switch architecture with only two stages comprising smaller (full) switch fabrics, and one with only FWCs. The FWCs are in fact switches that switch in the wavelength domain. A cost evaluation of this 2-stage design can be found in [13] and is beneficial in almost the entire practical parameter space.

### B. *The AWG based architecture*

In section II.B we discussed a non-blocking AWG based switch. Key component there is a TWC that can tune over the entire range *F.W*. When large switches are needed this could become infeasible. Furthermore the used AWGs become quite big. Thus, it can be interesting to use a Clos 3-stage design, shown in Fig. 6. We see that, with the chosen design parameters, all outputs of an output stage go to one output fibre, thus we can again replace that stage with FWCs. Note that we have used 2.*W* middle stages. 2.*W*-1 would suffice, but 2.*W* allows for more conventional AWG sizes.

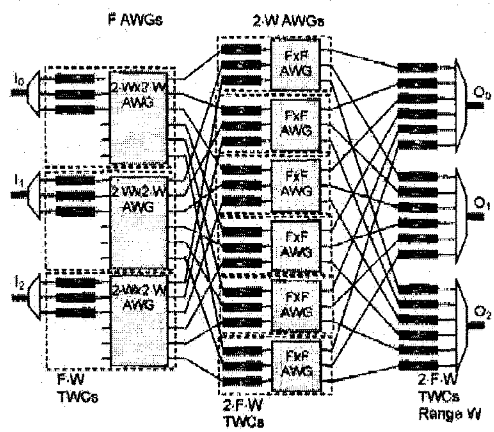


Fig. 6 Two- stage design for an AWG based switching node.

## IV. Upgrading Multistage Nodes

The above discussed multistage nodes can be used in an environment of traffic growth. The main objective is to only install parts of the switch when they are needed, so that investments can be spread in time, and overall costs can be reduced.

### A. *Clos nodes*

In a traditional 3-stage Clos node design, the middle stage needs to be completely built from the start. Exception is the trivial case when only one $1^{st}$ (and one $3^{rd}$) stage is present. The blocks in the $1^{st}$ and $3^{rd}$ stage can be installed at the moment they are needed. Suppose we have a non-blocking 3-stage NxN Clos switch, with N/n input blocks of size *nx(2.n-1)*, 2.n-1 *N/nxN/n* stages and N/n output stage blocks of size *(2n-1)xn*. The 2.n-1 middle stages must be present from day one, while the outer stages can be built out as needed, by adding outer blocks of size *nx(2.n-1)* and *(2.n-1)xn* as traffic demand grows. We call these upgrades *small upgrades*. When all N/n of these outer blocks are present the Clos node is completely built, and upgrades are then only possible if the middle stage is also changed. One way of doing this is by making a g.Nxg.N switch: use larger outer blocks, say of size g.nx2.g.n-1, this means we need 2.g.n-1 middle stages of size N/n, which means the 2.n-1 ones that were already installed can be reused. For this kind of upgrade we use the term *large upgrades*.

Special attention is needed for the AWG based node. We stated that the middle stage needed to be completely built out for the Clos case, well there is an important nuance for the AWG based approach. In this kind of node the switching itself happens in the AWG, but it is the TWC that governs the switching. The state of the AWG never changes, it is the setting of the TWC that allows the whole to function as a switching matrix. This means that the central stage AWGs need to be all present from the beginning. However, the TWCs between the 1st and the 2nd stages can be added at the moment the input blocks are installed. The same logic holds for the input block.

In a B&S node the input block is immediately entirely placed. Using the AWG based approach we only need to install TWCs at the inputs of wavelengths that are active, the other inputs of the AWG do not need their TWC. The TWCs at the output of the input blocks do all need to be present, as they control the switching in the 2nd stage.

So in summary when an input block is installed, all its output ports need to have TWCs (which are the TWCs at the input of the middle stage), and the input ports of the input blocks needs TWCs on the wavelength channels that are active. These active wavelengths are determined via a network dimensioning, see section V.A.

### B. The SKOL technique

Mc Donald presents some interesting thoughts on Clos switches and modifies the design, such that it is changed into just input and output blocks, which are in fact identical when a reciprocal technology is used [14]. This would allow for a cost reduction due to economy of scale, and an improved upgrade situation. We summarize his method here logically in Fig. 7: split up the switching functionality of the middle stage and distribute it into the outer blocks. The 2.n-1 middle stages, which consisted of N/nxN/n switches are now included in the 1st (3rd) stage in the form of 2n-1 1xN/n (N/nx1) switches.

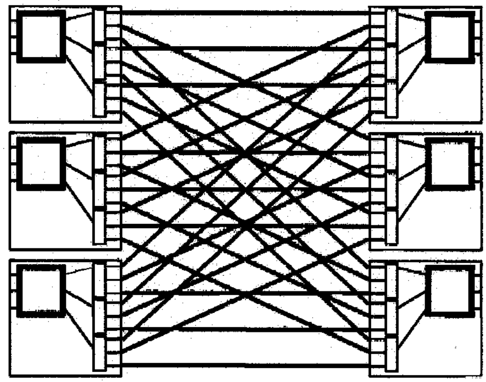

Fig. 7 Logical representation of the SKOL technique: distribute the middle stage functionality over the 2 outer stages.

Upgrading in the SKOL approach means that extra input/output blocks are installed: this again is the so called *small upgrade*. The eventual maximum achievable size is determined by the size of the distributed middle stage, so the same limit holds as for the Clos approach. However when we want to let the size of the switch increase even further, we need to remove all the SKOL blocks and start all over, no reuse is possible as was the case in the Clos architecture. This is the *large upgrade*.

We have used this SKOL technique on both the OPS architectures described in Section II in [15] and shown that for the B&S node architecture, it can be beneficial to use this SKOL technique under the condition that a cost reduction in function of time is taken into account. For the AWG based design however, SKOL does not help.

### C. Using wavebands for more flexibility

Section III explains the 3 stage Clos design could be simplified to a 2 stage design, when the outputs of the 3rd stage all went into the same fibre. We like to stress here that this does not mean that one outgoing 3rd stage should correspond to one outgoing fibre. More than one outgoing block can go into one output fibre. Key is that outputs of the same output block do not go into different fibres, as then the switching functionality in the 3rd stage is not limited to the choice of a wavelength. This allows using these 2-stage approaches in the upgrade scenarios. In the upgrade scenarios discussed here, we will assume a fixed fibre topology, so *F*, the number of fibres, will never change. We will do upgrades not on a per wavelength level, but when an upgrade is required an extra block is immediately installed, so a number of wavelengths. The size of these blocks of course impacts the cost of the switch, as it determines the granularity of the upgrade.

### D. Bit rate transparency

As we are dealing with OPS, we assume that node architectures are transparent to the bit rate of the signals going over the wavelengths. In other words any data bit rate can be switched through the nodes: no additional cost is present to let the switches operate at higher data speed. There is however a cost at the ingress of the network where packets get Electro-Optically converted and sent out. Those transceivers have higher cost for a higher bit rate. We will discuss this cost further in section V.B.

## V. Methodologies Used

### A. *Network scenario*

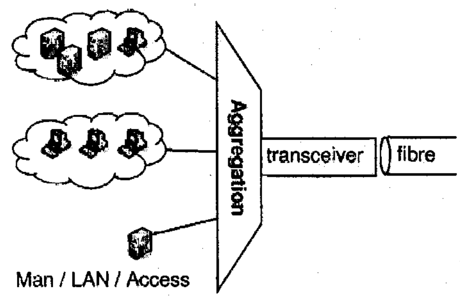


Fig. 8 Edge node functionality illustrated.

Fig. 8 shows a brief description of the networking scenario, focusing on the edge functionality. Traffic coming in from Metropolitan/Local Area Network(s), or server sites, is all aggregated electronically in the edge part of an OPS node. The aggregated traffic is then sent over the fibre using a transceiver. When talking about transceivers in the remainder, consider a scenario as in Fig. 8. These nodes are then used in a network, as shown in Fig. 9.

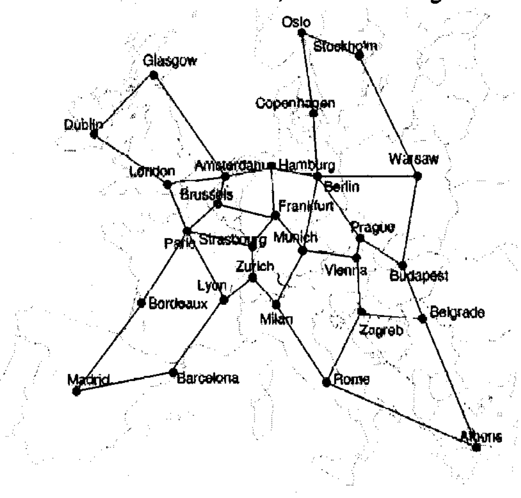


Fig. 9 Pan-European network used for network dimensioning.

For our study we used a Pan-European network shown in Fig. 9, using realistic traffic demands [4]. We used commercial dimensioning software [16] to evaluate the traffic on the different links. We performed this evaluation for different bit rates: 2.5 Gb/s, 10 Gb/s, 40 Gb/s, 80 Gb/s and 160 Gb/s.

### B. *Cost functions used*

As we try to evaluate the cost of the different upgrades, we need to say some words on how we evaluate the costs of different nodes. First of all we need to stress that it is very hard to put some absolute, realistic numbers on the costs of components such as TWCs, as they are still very much in a research phase. Therefore we have to use simple models that can already provide us with some basic insights. As components would mature and their cost functions become clear, more detailed numbers could be used as input.

For the B&S node, we count the number of SOAs in the node, as these would be dominating the cost [13]. For the AWG based node we can use the TWCs (and FWCs), again because these will surely dominate over the cost of a passive AWG. For the transceivers (see Fig. 8), we use a commonly used rule of thumb: when capacity goes up by a factor of 4, the cost rises by a factor of 2.5 [17].

### C. *Cost erosion*

In our study we also let the factor cost erosion come into play: a component's cost today will be higher than the cost one year later. Let $C_i$ be the cost i years after the reference year, the cost in the reference year is the $C_0$, while $p$ denotes the price drop in 1 year. So if $p$=0.1, this means that there is an annual price reduction on 10%. We use a simple yet quite realistic exponential model [18]:

$$C_i = C_0.(1-p)^i \quad (1)$$

We use the same cost erosion $p$ for all the optical components, as both SOAs and TWC rely on the same basic material technology.

## VI. Studied Upgrade Scenarios

We will now look at multistage node upgrades from some different viewpoints. In all cases we study the cost of the entire network: first the network is dimensioned, i.e. we find out what capacity needs to be installed on all links. Then we use this info to calculate the cost (and evolution of this cost) of the individual nodes. We will always look at cumulative cost: the total amount of money spent at the end of the observed period. We start in A by giving some insight in what happens in a single node as traffic grows. In B and C we look into network wide costs, respectively for the B&S and the AWG based node design, without bit rate upgrades. D and E describe 2 different scenarios using bit rate upgrades.

*A. Single node*

In Fig. 10 we show the cumulative cost evolution for a single B&S multistage node, comparing a Clos an SKOL approach. The maximum size of this switch (the size when it is completely built out) has 10 input blocks. The node starts out with 1 input block in place, and every year an output block is added. When no cost erosion is taken into account, the cost of the SKOL architecture starts out cheaper but in the end the Clos design is beneficial. However with a cost erosion of 15 % the SKOL architecture is the cheapest one, as every year the upgrade cost less. We clearly see the importance of taking cost erosion into account.

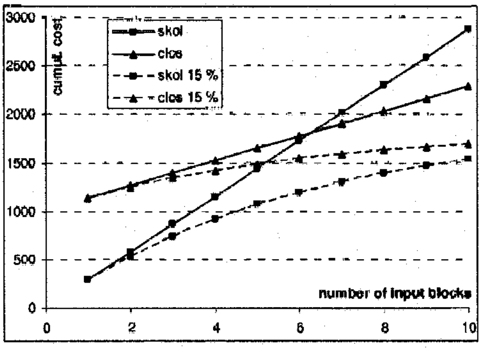


Fig. 10 Cumulative cost evolution for a B&S multistage node, starting with 1 input block, adding 1 input block every year.

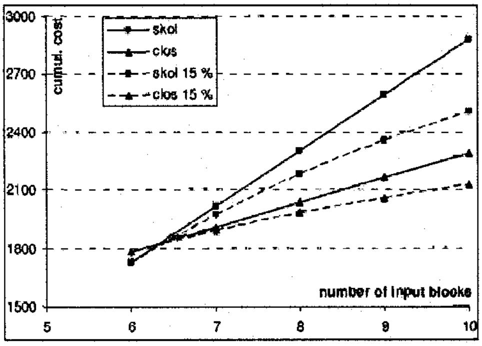


Fig. 11 Cumulative cost evolution for a B&S multistage node, starting with 6 input blocks, adding 1 input block every year.

In contrast with this result we see on Fig. 11 that when the initial build out of the same node is more substantial. The Clos and SKOL variants have almost the same cost. There is no realistic cost erosion possible that can make the SKOL variant beneficial in the end. So for the B&S variant there is no clear winner between Clos and SKOL, a lot is dependent on how large the initial switch is built out and the cost erosion. Thus small initial switches give an advantage to SKOL, when reasonable cost erosion is present.

The effects of small and large upgrades are shown in Fig. 12, where the evolution of the cumulative cost for the Brussels node is shown. taken out of a case study at 40 Gb/s described in B, with a cost erosion of 30%, a minimum band size of 32 and a middle switch size of 16, the growth factor was 2 (for details on what these parameters are, see the next section). Up to 2007 the growth in traffic can be handled with small upgrades, and we see SKOL is the most cost-effective approach until then. However if we want the switch to last longer, large upgrades become necessary. It is very clear that the large upgrade has as a consequence that the SKOL cost shows a steep rise. For all cases we studied, when a large upgrade was necessary the SKOL technique was never beneficial.

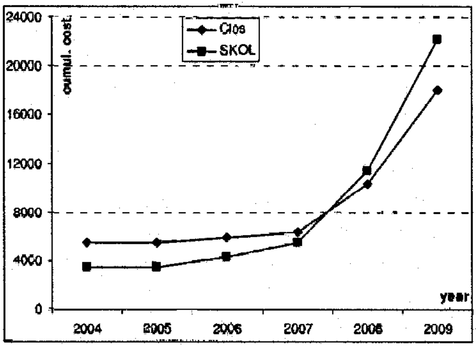


Fig. 12 Effects of small and large upgrades: SKOL design overtakes Clos design.

*B. Network wide, using B&S nodes*

We start by showing the evaluation for the Clos nodes, after which we look into the SKOL approach.

*1) B&S Clos*

We now extend our view onto the entire network, not just onto a single node. How does cost evolve when traffic grows and switches need upgrades? Which solutions are more cost-efficient than others? We will not use bit rate upgrade here, so the bit rate is fixed for the entire dimensioning period. We have already discussed the parameter of cost erosion $p$ in Section V.C, we will now discuss three more parameters we used in order to evaluate the cost evolutions of the rearrangeable non-blocking B&S switch.

- Minimum band size: the minimum band size used in any node in the network, as explained in section IV.C.
- Middle switch size: the size of the middle stage switching blocks. Note that this is also the maximum number of input blocks that can be present. Looking at a middle stage block in Fig. 5, there is exactly one input port from every input block. This can also be deducted from the condition for a rearrangeable non-blocking switch.
- Growth factor $g$: the growth factor applied when the traffic matrix can no longer be fulfilled with the used

band size (and the number of middle stage blocks, as this is equal for the rearrangeable non-blocking case). It denotes the extent of the large upgrade.

We dimension the network using the demand matrix. Then, for each node, we evaluate how many input blocks are needed, using the current band size. We check whether this number fulfills the condition of rearrangeability, i.e. the number of input blocks shoul not be larger than the maximum number. If this condition is not fulfilled the bands grow by a factor $g$, and the condition is checked again. We start with discussing the Clos multistage B&S OPS node.

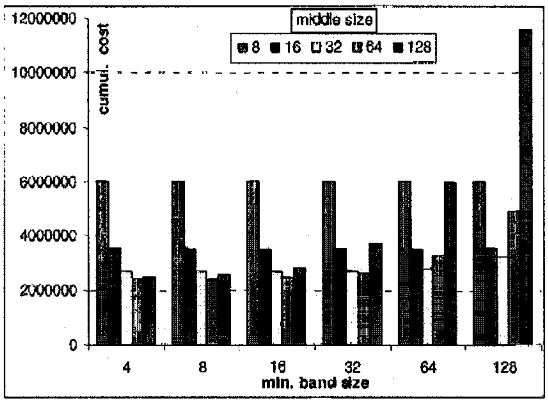


Fig. 13 Clos B&S. The cumulative cost in the final year (2007) using $g$=2 and $p$=0.15, bit rate was 2.5 Gb/s.

TABLE I
EVOLUTION OF THE AMSTERDAM NODE

| Year | Band size | Number of input blocks |
|---|---|---|
| 2004 | 32 | 25 |
| 2005 | 64 | 23 |
| 2006 | 128 | 26 |
| 2007 | 256 | 28 |

The results for a dimensioning at 2.5 Gb/s are shown in Fig. 13. The larger the minimum band size is chosen, the larger the cost. This is a matter of granularity: in the case the minimum band size is 128, even for a single wavelength a whole block of 128 wavelengths is needed. This happens from the start. In scenarios with a lower minimum band size, the end configuration also contains such large input blocks, certainly when the middle stage is not too large, however they only appear later, when traffic is large enough to justify them, thus cost erosion makes them cheaper. Table I illustrates this for the Amsterdam node, using a minimum band size of 32, $g$=2, $p$=0.15, and a middle size of 32 (like in Fig. 13).

For the middle sizes the story is not that straightforward: an intermediate value seem useful. A larger value allows postponing large upgrades, but too large values result in too large a central stage, which is not completely used in the end. In Fig. 14 the cost erosion is increased to an unrealistic 60 %, allowing us to have a low effect of late upgrades. We see the optimum values shift to smaller middle sizes, as large upgrades now have very low weight in the cumulative cost function. Note that when smaller input blocks are possible (low minimum band size) the optimum value of the middle size lies higher, as more input blocks need to be present for the same amount of traffic, and thus require a larger middle stage.

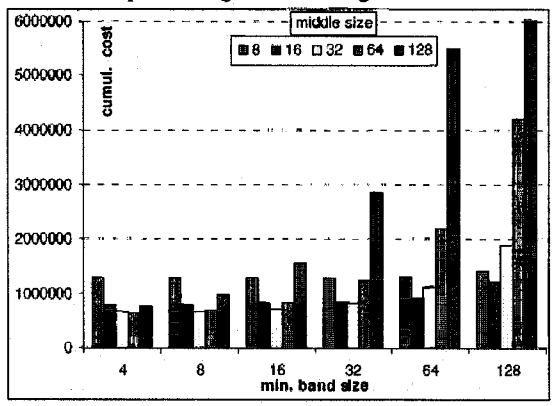


Fig. 14 Clos B&S. The cumulative cost in the final year (2007) using $g$=2 and $p$=0.6, bit rate was 2.5 Gb/s.

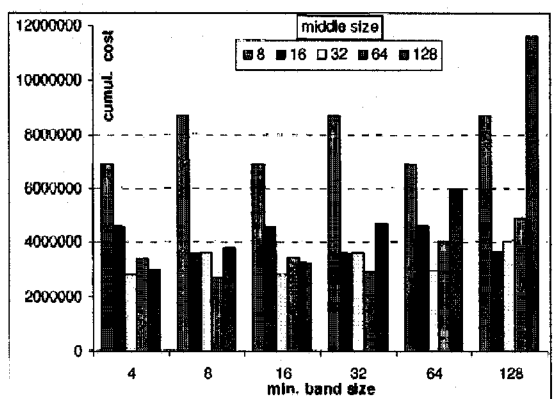


Fig. 15 Clos B&S. The cumulative cost in the final year (2007) using $g$=4 and $p$=0.15, bit rate was 2.5 Gb/s.

When a larger value of $g$ is used ($g$ is doubled in Fig. 15 compared to Fig. 13) the cumulative cost is never lower than with a smaller value for $g$. A larger $g$ value means a larger sudden increase of the node, more specific the middle stage (that must be completely built at the time of the large upgrade) is responsible for a sudden cost increase. It is clear that this sudden cost increase should be kept as low as possible. This is of course dependent on the traffic growth itself. In the traffic trace we used each year the traffic is 2.5 times larger than the year before, a large growth scenario. So when there is insufficient capacity an upgrade with a factor close to 2.5 intuitively seems quite a good one, which is confirmed by the two aforementioned graphs.

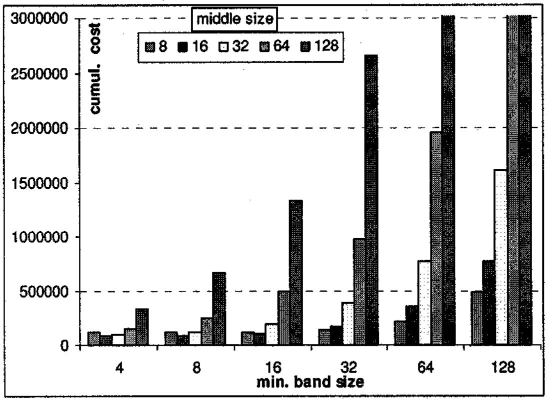


Fig. 16 Clos B&S. The cumulative cost in the final year (2007) using $g$=2 and $p$=0.15, bit rate was 40 Gb/s (note that some values are out of scale for a better visibility of the low values).

Finally, we look at the effect of bit rates in Fig. 16, where bit rate is increased to 40 Gb/s. This is done for all the dimensioned years, so no bit rate upgrade is done. It only shows the effect of switching granularity. First of all it is obvious that the cumulative cost can be substantially lower than in the 2.5 Gb/s case. The cost for the optimum values has a ratio close to 30, which is even larger than the factor 16 increase in bit rate. A wavelength now carries 16 times the amount of traffic, so the switch port count is indeed smaller.

As less input blocks can be expected the middle stage doesn't need to be as large as in the low bit rate case: the optima lie lower. Only when very small input blocks can be used (thus more of them will be present) we need somewhat larger middle stages.

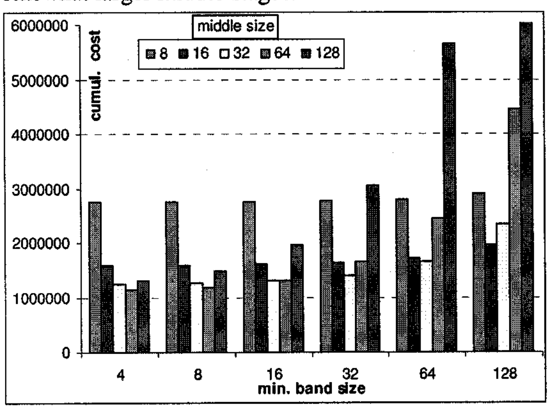


Fig. 17 Clos B&S. The cumulative cost in the final year (2010) using $g$=2 and $p$=0.15, bit rate was 40 Gb/s (note that some values are out of scale for a better visibility of the low values).

When we let the case of 40 Gb/s evolve even further in time, to 2010, the picture again changes, as in Fig. 17. More input blocks will be needed, so the optimum number of middle stages shifts to larger values.

*2) B&S SKOL*

We are interested whether the SKOL approach can result in switches that are more cost efficient when upgrades are needed. Results for the same parameters as in Fig. 13 are depicted in Fig. 18, but now based on the SKOL design.

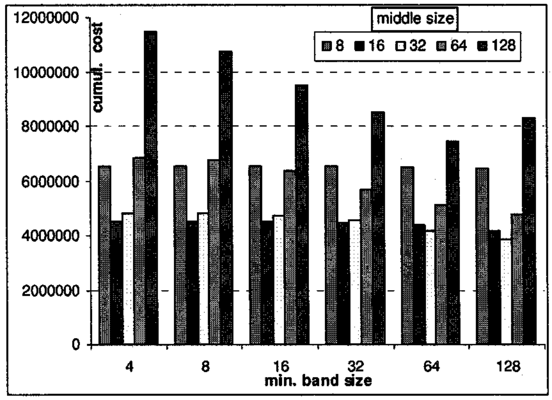


Fig. 18 SKOL B&S. The cumulative cost in the final year (2007) using $g$=2 and $p$=0.15, bit rate was 2.5Gb/s.

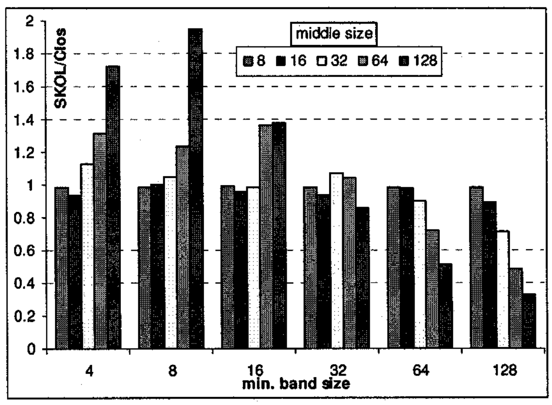


Fig. 19 The ratio of the cumulative cost of SKOL over Clos, in the final year (2007) using $g$=8 and $p$=0.6, bit rate was 2.5Gb/s.

Only in the case of very large minimum band sizes there is an advantage in using SKOL. In those cases the switch is only very sparsely used (has a low number of input blocks) in the beginning and no or few large upgrades are necessary (cfr. VI.A). Even when a larger cost reduction is used, the SKOL mechanism is only beneficial when the middle stage size is large and especially when the minimum band size is large. In Fig. 19 we show the extreme case (i.e. most beneficial for SKOL) where cost erosion $p$=60% and growth factor $g$=8. In quite a large part of the studied parameter space SKOL can have some positive effect. The reason is again that large upgrades will be sporadic and the nodes will be sparsely built in the beginning. However mostly the gain using SKOL is limited, and we need to mention that the optimum values in this case are a minimum band size of 4, with a middle stage size of 32. Thus in the optimum point Clos is still the winner. The effect of increasing bit rate is very similar to this, as it results in the same effects, less large upgrades and sparse switches at the beginning.

*C. Network wide, using AWG based nodes*

Looking at the cost for an AWG based Clos node, we see a different story. Large middle sizes are interesting when a high port count is present, which is the case at a low bit rate (2.5 Gb/s in Fig. 20).

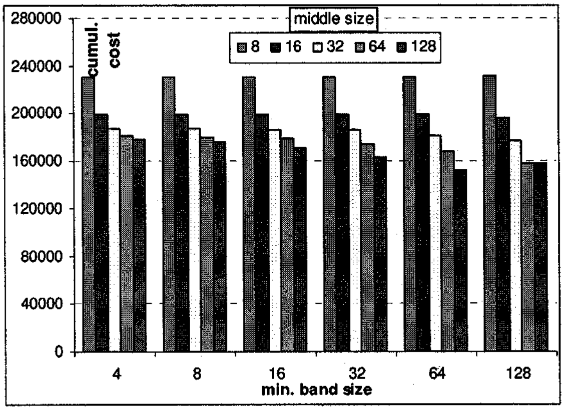


Fig. 20 Clos AWG based. The cumulative cost in the final year (2007) using $g$=2 and $p$=0.15, bit rate was 2.5Gb/s.

For the explanation we refer to IV.A: we can build out the middle stage with TWCs as needed, only the AWGs need to be present. This clearly favors large middle stages, as their installation from the beginning doesn't bring a large initial cost with them, which was the case for the B&S node design. For a minimum band size of 128, the cost of a 64 middle size and a 128 middle size has an equal cumulative cost. This can also be explained by this feature of the AWG based switch. The number of input blocks needed from 2004 to 2007 are 7, 12, 26 and 54 respectively, never more than 64. So a 64 sized middle stage is sufficient. Although a 128 sized middle stage is too large, as the TWCs are only installed as needed, there is no cost penalty, since the TWCS at in- and output of the input block determine the cost.

When minimum band size is too high, there are too much TWCs before the middle stage (i.e. at the output ports of the input block), which must be installed the moment the block is installed. On the other hand a low minimum band size results in very frequent large upgrades. The larger the cost erosion the less costly these upgrades become and smaller minimum band sizes could become interesting.

At higher bit rates (40 Gb/s in Fig. 21), large middle stages stay interesting as the TWCs can be added at the moment the corresponding. The shift of the optimum value towards lower minimum band size is because fewer wavelengths are present and thus the granularity of the bands needs to be finer. We again see that too large middle stages have no cost penalty as discussed before. The effect of too large minimum band sizes (too much TWCs are installed at the output ports of the input block) is more pronounced as less wavelengths are present, but with a higher data bit rate.

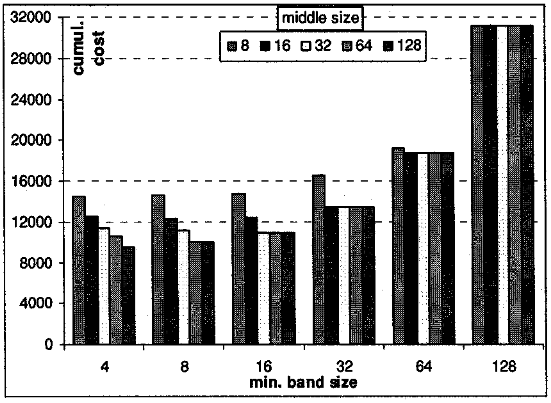


Fig. 21 Clos AWG based. The cumulative cost in the final year (2007) using $g$=2 and $p$=0.15, bit rate was 40Gb/s.

*D. Bit rate upgrades allowed, scenario 1*

Subsetions B and C did not take bit rate upgrades into account, now we include these. Here we will follow one approach, in the next section we present an alternative approach.

In the first approach we fix the band size and middle size for all nodes, so growth $g$ becomes irrelevant. Small upgrades are still used, however when a large upgrade would now be needed, we choose to increase the bit rate over the entire network. The available bit rates are: 2.5 Gb/s, 10 Gb/s, 40 Gb/s, 80 Gb/s and 160 Gb/s. It is possible that when a bit rate upgrade is done, the number of input blocks already installed is larger than the number strictly required. In that case we leave these input blocks. As stated in IV.D, we assume the OPS switch matrix technology is bit rate transparent, so no extra node cost is present when only a bit rate upgrade is done. This does not hold for the transceivers at the edge of the OPS network, which inject the optical packets into the network. They do have an additional cost when bit rate is increased, we use the rule of thumb that the cost increases by a factor of 2.5, when speed goes up by a factor of 4. For the transceiver we assume a cost erosion of 15% per year. We stated how this cost is handled in section V.B, we also introduce the ratio *r*:

$$r = \frac{Transceiver 2.5Gb/s[in 2004]}{SOA\,cost[in 2004]} \quad (2)$$

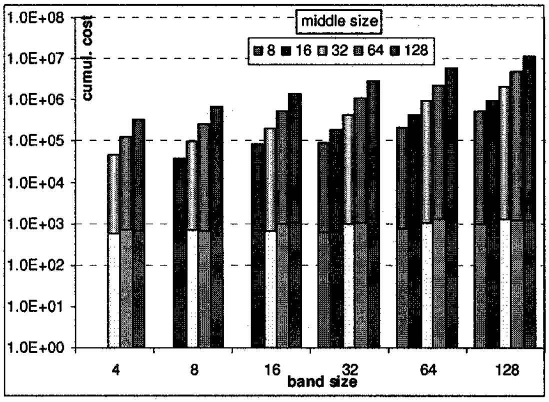


Fig. 22 Clos B&S. Cumulative cost in the final year (2007); *r=0.1 and p=0.15*. Missing values indicate the traffic could not be handled with the given possibilities. The lower bars indicate transceiver cost, the upper ones switching node cost.

Fig. 22 shows that switches with small building blocks are the most cost effective: optimum band size is 8 and middle stage size is 16. The switch starts in 2004 at 40 Gb/s, in 2006 an upgrade to 80 Gb/s is necessary and in 2007 160 Gb/s is needed. Notice that switches with very small blocks are not possible with the bit rates available in this study. We have split up the costs in a transceiver part and a switch part. We see the transceiver part is virtually not contributing to the total cost picture (logarithmic scale!!!). Note that this means that considering even smaller values of *r* will have no effect.

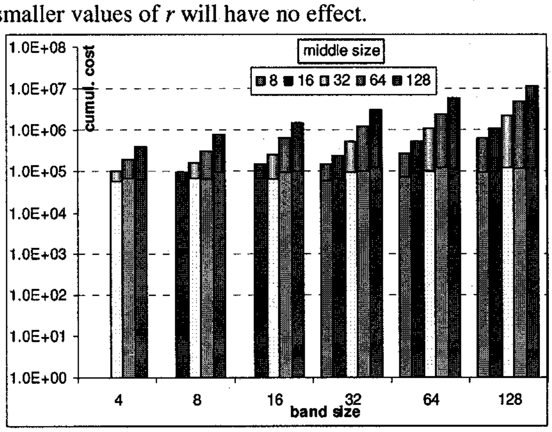


Fig. 23 Clos B&S. Cumulative cost in the final year (2007); *r=10 and p=0.15*. Missing values indicate the traffic could not be handled with the given possibilities. The lower bars indicate transceiver cost, the upper ones switching node cost.

We see the influence of the ratio *r* in Fig. 23, *r* is increased with two orders of magnitude to *r*=10. The relative importance of the switch matrix cost decreases. For the smaller values for the band size and the middle stage size, the transceiver cost starts to have an influence we can no longer neglect. Using larger values of band size and middle size, the switch portion is still dominating. The optimum parameters values are still the same.

However when *r*=100, when transceivers would be extremely more expensive than a SOA, the weight of the transceivers is considerably high for almost all cases and the optimum value shifts towards a larger band size, i.e. 32, as we see on Fig. 24, while small middle sizes stay preferable. The larger band size has as a consequence that bit rates are lower. In 2004 and 2005 10 Gb/s is used, while the next two years are serviced at 40 Gb/s. So using the, now relatively expensive, higher speed transceivers is postponed until their cost has dropped sufficiently due to the cost erosion.

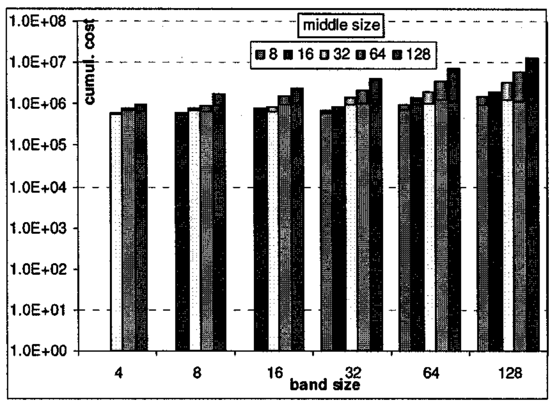


Fig. 24 Clos B&S. Cumulative cost in the final year (2007); *r=100 and p=0.15* Missing values indicate the traffic could not be handled with the given possibilities. The lower bars indicate transceiver cost, the upper ones switching node cost.

The SKOL case is very similar to the Clos case, in fact the same optimum values for the parameters are found. However, as large upgrades are never needed, we expect the SKOL mechanism to be more powerful here than it was without bit rate upgrades. This is illustrated in Table II, where for low or medium values for *r*, the SKOL approach does give a benefit over the Clos OPS node design. We see a 10 to 15% gain can be reached, when a transceiver is cheaper than a SOA. However when transceiver cost is remarkably higher than SOA cost, there is almost no gain left, which is logical as the transceiver cost is equal for the Clos and SKOL case, and it governs the total cost when transceiver cost dominates SOAs.

In Fig. 25 we show evolution in time of the cumulative cost for $r$=0.1 and in Fig. 26 for $r$=10. Although the case with the smaller switch blocks uses higher bit rates earlier on in time, it has a lower transceiver cost contribution. This is due to the adopted realistic model of V.B, a capacity increase of a factor 4, only implies a 2.5 cost increase.

TABLE II

COST RATIO OF SKOL OVER CLOS, FOR DIFFERENT $r$ VALUES

| r | Skol/Clos |
|---|---|
| 0.01 | 0.8455 |
| 0.1 | 0.8476 |
| 0.25 | 0.8510 |
| 0.5 | 0.8565 |
| 1 | 0.8661 |
| 2 | 0.8820 |
| 4 | 0.9047 |
| 10 | 0.9396 |
| 100 | 0.9907 |

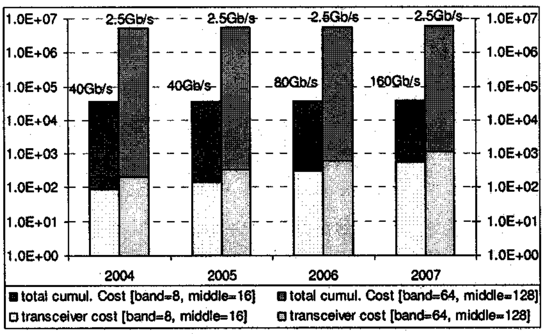


Fig. 25 Cumulative cost evolution in time, $r$=0.1.

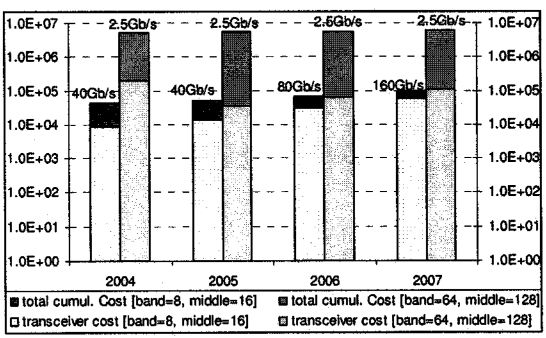


Fig. 26 Cumulative cost evolution in time, $r$=10.

## E. Bit rate upgrades allowed, scenario 2

A second scenario we use to study the effect of bit rate upgrades, is one where we fix the bit rate upgrade moments. We use the values depicted in Table III. With these bit rates in place we use the same strategy as followed in B: we let the switch grow using small and large upgrades. But at the points in time indicated in Table III, we let the bit rate increase. This also re-introduces the usage of small and large upgrades. Again we use the cost ratio $r$ from (2), as we need to take the cost for these bit rate upgrades into account. However the most ideal configurations seem to be independent of the value of this $r$, even when $r$ varies over 4 orders of magnitude from 0.01 to 100. Main reason for this is the high amount of SOA's totally governing the cost. For the following graphs we used a value of $r$=1.

TABLE III

THE USED BIT RATES IN EACH YEAR

| Year | Used bit rate [Gb/s] |
|---|---|
| 2004 | 2.5 |
| 2005 | 2.5 |
| 2006 | 10 |
| 2007 | 10 |
| 2008 | 40 |
| 2009 | 80 |
| 2010 | 160 |

Fig. 27 shows we don't want large band sizes, this is for granularity purposes. The middle stage however should be large enough, avoiding (frequent) large upgrades. It should however not be too large, as this results in a middle stage so big that it is never entirely used. Because of the bit rate upgrades we do no longer need a very high port count, explaining the lower middle stage size compared to e.g. Fig. 13. Optimum values are a minimum band size of 4 and a middle size of 32 for this case.

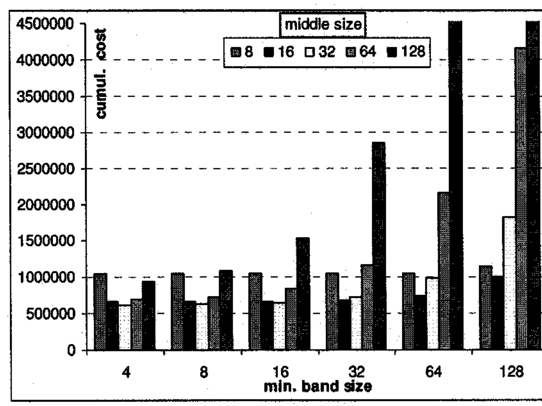


Fig. 27 Clos B&S. Cumulative cost in the second bit rate upgrade scenario, $r$=1, $g$=2 and $p$=0.15 (some values out of scale for clarity of the whole picture).

For the SKOL architecture trends are somewhat different, Fig. 28. Again an intermediate value for the middle size is good, however a slightly smaller one seems preferable in the SKOL architecture. At the same time, minimum band size has hardly any influence. Optimum values here are a band size of 64 and a middle stage size of 16.

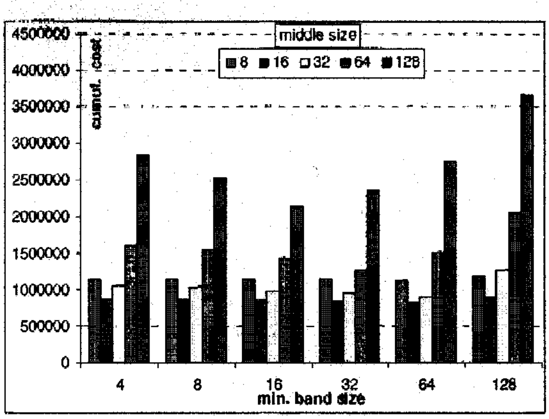


Fig. 28 SKOL B&S. Cumulative cost in the second bit rate upgrade scenario, r=1, g=2 and p=0.15.

We compare the SKOL architecture and the Clos architecture in Fig. 29. Only for large minimum band sizes the SKOL approach is relatively beneficial, however in the parameter space where SKOL is beneficial the absolute cost of the Clos design is far from ideal, which explains the values lower than 1 in Fig. 29 and can also be deducted from the comparison of Fig. 27 and Fig. 28.

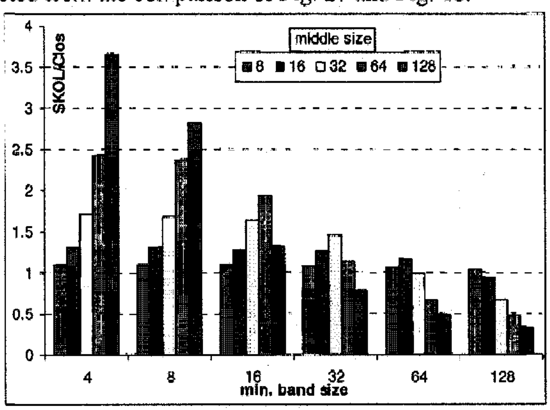


Fig. 29 Comparison between SKOL and Clos in the second bit rate upgrade scenario, $r$=1, $g$=2 and $p$=0.15.

## VII. Conclusion

We have studied approaches to the upgrading problem in an OPS environment. We showed that Clos and its variant the SKOL design are upgradeable designs. We also introduced the concepts of using bands of wavelengths, in order to be able to continue using the 2-stage OPS nodes. Without bit rate upgrades there is a large cost increase when a large upgrade is needed, therefore this should be postponed in time, as cost erosion makes this cheaper. Without bit rate upgrades the SKOL architecture can never outperform the Clos architecture. However allowing bit rate upgrades in optically transparent OPS nodes can give SKOL an advantage. Furthermore an AWG based node Clos design is well suited to use in upgrading. The switching core, the AWG, is a simple passive device, TWCs on the interfaces toward the AWG ports actively govern the switching, but are also the dominant cost factor in that kind of node design. Especially the middle stage has an interesting property, although overdimensioned, it does not bring a supplementary cost, so one should install large AWGs for the middle stage.

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